**In the claims:**

1. Canceled

2. Canceled

3. (Previously presented) The system of claim 32, wherein the BIST controller includes an interface to receive one or more additional memory test algorithms, wherein the algorithm controller delivers the additional memory test algorithm to the sequencer for application to the memory interface.

4. Canceled

5. (Previously presented) The system of claim 32, further comprising a set of command data interconnects to communicate the commands from the BIST controller to the plurality of sequencers and a set of acknowledgement interconnects to communicate acknowledge signals from the plurality of sequencers to the BIST controller to indicate the completion of the commands.

6. (Previously presented) The system of claim 23, wherein the sequencer controls an application speed of the memory operations to the memory interface in accordance with timing requirements of the memory module.

7. (Previously presented) The system of claim 23, wherein the sequencer comprises:

a plurality of command controllers that implement the commands in accordance with a command protocol; and

a command parser to parse each command to identify an operational code and a set of parameters based on the command protocol, wherein the command parser selectively invokes the command controllers based on the operational codes of the commands received from the BIST controller.

8. (Previously presented) The system of claim 7, wherein when invoked the command controllers issue the memory operations to the memory interface by sequencing through address ranges defined by the respective commands.

9. (Original) The system of claim 7, wherein the command controllers issue the memory operations by asserting signals to apply addresses and data to the memory interface based on the commands received from the BIST controller.

10. (Previously presented) The system of claim 9, wherein the command controllers issue the memory operations by further asserting control signals to direct the memory interface to automatically store inverted data between at least one of neighboring rows, neighboring columns, and neighboring row-column matrices based on the physical characteristics of the memory module.

11. (Original) The system of claim 9, wherein based on the physical characteristics of the memory module the memory interface translates the addresses specified by the sequencer for the memory operations.

12. (Original) The system of claim 11, wherein the memory module includes memory cells arranged in rows and columns, and the memory interface translates the addresses to fill the memory module in a row-wise or column-wise fashion as specified by the commands from the BIST controller.

13. (Original) The system of claim 9, wherein the commands specify a bit pattern to be written to the memory module, and the memory interface translates the data specified by the sequencer based on the specified bit pattern and the physical characteristics of the memory module.

14. (Previously presented) The system of claim ~~1~~ 23, wherein the memory interface comprises a data generation unit that receives data signals from the sequencer and generates transformed data signals based on the data signals and the physical characteristics of the memory module.

15. (Original) The system of claim 14, wherein, in response to a control signal received from the sequencer, the data generation unit automatically transforms the data to store inverted data within at least one of neighboring rows, neighboring columns, and neighboring row-column matrices of the memory module.

16. (Previously presented) The system of claim 23, wherein the memory interface comprises an address generation unit that receives address signals from the sequencer and generates transformed address signals applied based on an arrangement of rows and columns of the memory module.

17. (Previously presented) The system of claim 23, wherein the memory interface comprises a comparator to compare data read from the memory module to data previously written to the memory module and set a state of a failure signal based on the comparison.

18. (Previously presented) The system of claim 23, wherein the physical characteristics include at least one of a number of rows, a number of columns, and a number of row-column matrices of the memory module.

19. (Previously presented) The system of claim 23, wherein the commands conform to a generalized command protocol that substantially defines the test algorithm without regard to physical characteristics and timing requirements of the memory module.

20. (Original) The system of claim 19, wherein the command protocol defines a command syntax having a set of supported commands, and each command includes an operand and a set of parameters.

21. (Original) The system of claim 20, wherein at least one of the commands includes fields to specify an address range, one or more memory operations to apply over the address range, and a bit pattern for application to the memory module of the address range.

22. (Previously presented) The system of claim 23, wherein the BIST controller, memory interface and sequencer are integrated within an electronic device.

23. (Previously presented) A system comprising:

a plurality of memory modules, at least one memory module having a clock domain different that other of said plurality of memory modules;

a single built-in self-test (BIST) controller that stores an algorithm for testing the memory modules; and

a plurality of sequencers, each sequencer coupled to a different subset of the memory modules, wherein each subset of the memory modules is selected to include the memory modules having common clock domains, and each sequencer controls the application of the test algorithm to the respective subset of memory modules in accordance with the common clock domain of that subset of memory modules.

24. (Previously presented) The system of claim 23, further comprising a plurality of memory interfaces that are respectively coupled to the memory modules, wherein each of the memory interfaces receive address and data signals generated by the sequencer based on the algorithm and translates the address and data signals in accordance with an arrangement of rows and columns of the respective memory module.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Currently amended) ~~The system of claim 1~~ A system comprising:

a plurality of memory modules, at least one of the memory modules having physical characteristics different than other of said plurality of memory modules,

a single built-in self test (BIST) controller that stores a set of commands defining an algorithm for testing the plurality of memory modules;

a plurality of sequencers, each sequencer associated with a respective set of one or more memory modules that share common physical characteristics and operative to receive the commands and issue one or more memory operations in accordance with the commands; and

a plurality of memory interfaces, each memory interface operative to apply the memory operations to an associated memory module in accordance with physical characteristics of the memory module,

wherein the BIST controller comprises:

an algorithm memory that stores the set of commands as one of a set of selectable memory test algorithms having associated commands; and

an algorithm controller to retrieve the commands from the algorithm memory and issue the commands associated with the selected memory test algorithm to the sequencer,

wherein the algorithm controller issues each of the commands to the sequencers in parallel for application to the respective subsets of the memory interfaces

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